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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,888	02/01/2001	Jun Koyama	740756-2255	3194

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EXAMINER	
WEISS, HOWARD	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/774,888	Applicant(s) KOYAMA ET AL.	
	Examiner Howard Weiss	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 34-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 740756-2255

Filing Date: 2/1/01

Continuing Data: RCE established 3/27/03

Claimed Foreign Priority Date: 2/1/00 (JPX)

Applicant(s): Koyama et al. (Kato)

Examiner: Howard Weiss

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/27/03 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Initially, and with respect to Claims 1, 3, 45, 60 and 66, note that a "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al., 227 USPQ 964 (CAFC, 1985)* and the related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).*

Note that Applicant has burden of proof in such cases as the above case law makes clear.

4. Claims 1 to 12 and 34 to 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (JP 11-154714 and the Derwent Translation of this document), Akbar (U.S. Patent No. 5,656,845) and Chang et al. (U.S. Patent No. 5,471,422).

Yamazaki et al. show most aspects of the instant invention (e.g. Figures 1, 2 and 8) including:

- a memory cell array with memory cells formed in a matrix
- each cell containing a memory thin film transistor (MTFT) **Tr1** and a switching thin film transistor (STFT) **Tr2** said transistors integrally formed (Paragraph 0011 of Derwent)
- said MTFT including:
    - a first semiconductor active layer **202** formed on an insulating substrate **201** and having a first thickness **d1**

- a first insulating film **211**, a floating gate electrode **213**, a second insulating film **214** and a control gate electrode **215**
- a wiring **825** for connecting the control gate to a first single line **809**

- said STFT including:
  - a second semiconductor active layer **206** firmed on an insulating substrate **201** and having a second thickness **d2**
  - a gate insulating layer **212** and a gate electrode **217**
  - a second signal line **810** connected to said gate electrode
- where in **d1** is thinner (i.e. smaller) than **d2** and within the ranges claimed (Paragraphs 0058 and 0059)
- said first active layer connected to a third signal line **817** and the second active layer connected to a fourth signal line **818** and where said third and fourth signal lines are perpendicular to said first and second signal lines
- the various layers are formed in the same layer as claimed (Paragraph 0109)
- the memory cell array included in the devices claimed (e.g. Figure 12)

Yamazaki et al. does not show the first and second semiconductor layer in a common semiconductor island or at least two adjacent memory cells sharing a common signal line therebetween. Akbar teaches (e.g. Figures 1, 9 and 10) to form first and second semiconductor layers in a common semiconductor island (i.e. layer) **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a common semiconductor island as taught by Akbar in the device of Yamazaki et al. to provide memory cells with improved performance and reliability. Additionally, it is common, and therefore obvious, to form the third and fourth signal lines on top of the interlevel dielectric.

Chang et al. teach (e.g. Figure 5) to have at least two adjacent memory cells **40** share a common signal line **50** therebetween to overcome the problem of delayed

programming times without over-erase problems (Column 2 Lines 42 to 46). It would have been obvious to a person of ordinary skill in the art at the time of invention to have at least two adjacent memory cells share a common signal line therebetween as taught by Chang et al. in the device of Yamazaki et al. to overcome the problem of delayed programming times without over-erase problems.

Additionally, how the transistors of the memory cells are formed, either integrally or by some other means, or if various features (e.g. the floating gate electrode, the gate electrode, the first signal line and the second signal line) are formed of the same layer relates to intermediate process steps (i.e. "product-by-process") and does not affect the final device structure.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

   A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

   Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1 to 12 and 34 to 74 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 to 12 of copending Application No. 09/156,913 in view of Akbar and Yamazaki et al. (JP 11-154714 and Derwent Translation of this document). Application No. 09/156,913 claim most aspects of the instant except for the first and second

semiconductor layer a common semiconductor island and first to fourth signal lines connected as claimed.

Akbar teaches (e.g. Figures 1, 9 and 10) to form first and second semiconductor layers in a continuous layer **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). Yamazaki et al. teach (e.g. Figure 8) that is typical, and therefore obvious, to connect first to fourth signal lines **809, 810, 817, 818** as claimed, It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a continuous layer as taught by Akbar and to connect first to fourth signal lines as taught by Yamazaki et al. in the Device claimed in Application No. 09/156,913 to provide memory cells with improved performance and reliability and because it is a typical arrangement in the art.

This is a provisional obviousness-type double patenting rejection.

7. Claims 1 to 12 and 34 to 74 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 to 30 of copending Application No. 09/988,729 in view of Akbar and Yamazaki et al. (JP 11-154714 and Derwent Translation of this document). Application No. 09/988,729 claim most aspects of the instant except for the first and second semiconductor layer a common semiconductor island and first to fourth signal lines connected as claimed.

Akbar teaches (e.g. Figures 1, 9 and 10) to form first and second semiconductor layers in a continuous layer **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). Yamazaki et al. teach (e.g. Figure 8) that is typical, and therefore obvious, to connect first to fourth signal lines **809, 810, 817, 818** as claimed, It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a continuous

layer as taught by Akbar and to connect first to fourth signal lines as taught by Yamazaki et al. in the Device claimed in Application No. 09/988,729 to provide memory cells with improved performance and reliability and because it is a typical arrangement in the art.

This is a provisional obviousness-type double patenting rejection.

Response to Arguments

8. Applicant's arguments with respect to claims 1-12 and 34-74 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **-7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications. The official TC2800 Before-Final, **(703) 872-9318,** and After-Final, **(703) 872-9319**, Fax numbers will provide the fax sender with an auto-reply fax verifying receipt of their fax by the USPTO.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(703) 308-4840** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**.Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 Receptionist at **(703) 308-0956**.

11. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/326, 347; 365/ 185.05	thru 5/30/03
Other Documentation: none	
Electronic Database(s): EAST, IEL	thru 5/30/03

Howard Weiss
Patent Examiner
Art Unit 2814

HW/hw
30 May 2003